

*rule 1*  
*C2*  
7. (Twice Amended) A semiconductor device comprising:  
a semiconductor substrate;  
a MOSFET formed on the substrate;  
a signal input pad connected to a gate of the MOSFET, said signal input pad receiving  
an input signal for the MOSFET;  
a high concentration impurity diffused region located below the signal input pad and  
at a surface part of the semiconductor substrate;  
an interconnection connected to the high concentration impurity diffused region, said  
interconnection being electrically isolated from said signal input pad;  
a polysilicon layer provided just under said signal input pad, said polysilicon layer  
being connected to the interconnection, and  
a low resistance layer provided on the upper surface of the high concentration  
impurity diffused region and said polysilicon layer.

See the attached Appendix for the changes made to effect the above claim(s)

Please add the following new claim(s):

- rule 1*  
*C3*  
18. (New) The semiconductor device according to claim 1, wherein said signal  
input pad locates within an area of the high concentration impurity diffused region.
19. (New) The semiconductor device according to claim 7, wherein said signal  
input pad locates within an area of the polysilicon layer.